CLAIMS:

1. A receiver comprising:

an oscillator outputting phases of a clock signal; and

a retiming mechanism coupled to said oscillator having circuitry for receiving said phases of said clock signal, circuitry for receiving serial data, and circuitry operable to reduce timing uncertainties in said serial data by outputting a value of said serial data sampled at a particular phase of said clock.

2. The receiver as recited in claim 1, wherein said retiming mechanism comprises a plurality of first units, wherein each of said plurality of first units comprises circuitry for sampling said serial data using a particular phase of said clock.

3. The receiver as recited in claim 2, wherein each of said plurality of first units comprises circuitry for receiving said particular phase of said clock and a complement of said particular phase of said clock and said serial data.

4. The receiver as recited in claim 2, wherein said retiming mechanism further comprises a plurality of second units, wherein each of said plurality of second units is associated with a particular first unit, wherein each of said plurality of second units comprises circuitry for outputting a value of said serial data sampled by said associated first unit upon activation.

5. The receiver as recited in claim 4, wherein a particular second unit of said plurality of second units is activated based on a logical state of each input to said particular second unit.

6. The receiver as recited in claim 5, wherein said logical state of each input is determined based on combinational logic using said phases of said clock and complements of said phases of said clock.

7. A system comprising:

a transmission medium;

a transmitter coupled to said transmission medium configured to convert parallel data to a serial form; and

a receiver coupled to said transmission medium, where said receiver comprises:

an oscillator outputting phases of a clock signal; and

a retiming mechanism coupled to said oscillator having circuitry for receiving said phases of said clock signal, circuitry for receiving serial data, and circuitry operable to reduce timing uncertainties in said serial data by outputting a value of said serial data sampled at a particular phase of said clock.

8. The system as recited in claim 7, wherein said retiming mechanism comprises a plurality of first units, wherein each of said plurality of first units comprises circuitry for sampling said serial data using a particular phase of said clock.

9. The system as recited in claim 8, wherein each of said plurality of first units comprises circuitry for receiving said particular phase of said clock and a complement of said particular phase of said clock and said serial data.

10. The system as recited in claim 8, wherein said retiming mechanism further comprises a plurality of second units, wherein each of said plurality of second units is associated with a particular first unit, wherein each of said plurality of second units comprises circuitry for outputting a value of said serial data sampled by said associated first unit upon activation.

11. The system as recited in claim 10, wherein a particular second unit of said plurality of second units is activated based on a logical state of each input to said particular second unit.

12. The system as recited in claim 11, wherein said logical state of each input is determined based on combinational logic using said phases of said clock and complements of said phases of said clock.